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APPLICATION FOR LETTERS PATENT

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Methods of Forming Contacts, Methods of Contacting Lines, Methods of Operating Integrated Circuitry, And Integrated Circuits

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METHODS OF FORMING CONTACTS, METHODS OF CONTACTING LINES, METHODS OF OPERATING INTEGRATED CIRCUITRY, AND INTEGRATED CIRCUITS

TECHNICAL FIELD

This invention relates to methods of forming contacts, to methods of contacting lines, and to methods of operating integrated circuitry. The invention also relates to integrated circuits.

BACKGROUND OF THE INVENTION

Conductive lines which are utilized in integrated circuitry are often formed with widened areas called contact or landing pads. The purpose of these pads is to provide an extra degree of protection should a misalignment occur between a contact opening which is formed over the line. While advantages are gained in reducing the chances of a misalignment-induced failure, valuable wafer real estate is consumed by the widened pads.

Referring to Fig. 1, a portion of an exemplary prior art layout is shown generally at 10 and includes conductive lines 12, 14 and 16 having widened contact pads 18, 20 and 22, respectively. To conserve wafer real estate, it is usually desirable to provide conductive lines 12, 14, 16 to have a minimum pitch which is defined in large part by the minimum photolithographic feature size used to fabricate the circuitry. Minimizing the pitch of the lines ensures that the space between the lines, represented at S, is as small as possible. Yet, to

ensure that subsequently formed contacts to the conductive lines do not short to the substrate, the above-described widened contact pads are used. A design trade-off, however, is that in order to maintain a desired pitch between the conductive lines, and to avoid forming the contact pads too close together, the contact pads must necessarily be moved outwardly of one another. For example, in Fig. 1, contact pad 18 is moved outward in the direction of arrow A. Other contact pads can be spaced even further out depending on the dimensions of the contact pads. This results in consumption of valuable wafer real estate.

SUMMARY OF THE INVENTION

Methods of forming contacts, methods of contacting lines, methods of operating integrated circuitry, and related integrated circuitry constructions are described. In one embodiment, a plurality of conductive lines are formed over a substrate and diffusion regions are formed within the substrate elevationally below the lines. The individual diffusion regions are disposed proximate individual conductive line portions and collectively define therewith individual contact pads with which electrical connection is desired. Insulative material is formed over the conductive line portions and diffusion regions, with contact openings being formed therethrough to expose portions of the individual contact pads. Conductive contacts are formed within the contact openings and in electrical connection with the individual contact pads. In a preferred

embodiment, the substrate and diffusion regions provide a pn junction which is configured for biasing into a reverse-biased diode configuration. In operation, the pn junction is sufficiently biased to preclude electrical shorting between the conductive line and the substrate for selected magnitudes of electrical current provided through the conductive line and the conductive material forming the conductive contacts.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings:

Fig. 1 is a top plan view of a portion of a prior art circuit layout.

Fig. 2 is a diagrammatic side sectional view of a semiconductor wafer fragment in accordance with one embodiment of the invention.

Fig. 3 is a diagrammatic side sectional view of the semiconductor wafer fragment in accordance with another embodiment of the invention.

Fig. 4 is a top plan view of a circuit layout in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Figs. 2-4, separate embodiments of the present invention are shown and include a semiconductor wafer fragment generally at 24 (Fig. 2), 24a (Fig. 3) including a semiconductive substrate 26. Like numerals are utilized between the figures, with differences being indicated with the suffix "a" or "b", or with different numerals. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Substrate 26 comprises a first-type dopant which can be either p-type or n-type.

A plurality of conductive lines 28 are formed over substrate 26 and include a gate oxide layer 29, polysilicon layer 30, a silicide layer 32, an insulative cap 34, and sidewall spacers 36. Other conductive line constructions are possible. Diffusion regions 38 (Fig. 2), 38a (Fig. 3), and 38b (Fig. 4) are formed within substrate 26 and elevationally lower than conductive lines 28. In one embodiment,

dynamic random access memory (DRAM) circuitry is formed over and supported by substrate 26, with conductive lines 28 comprising individual word lines. DRAM circuitry typically includes storage cells which are disposed within a memory array, and a peripheral area proximate the memory array. The storage cells include a storage capacitor which is operably coupled with a word line through a diffusion region. Storage capacitors typically include a storage node layer, a dielectric layer, and a cell plate layer. The word lines extend through the memory array and the peripheral area proximate the memory array. Diffusion regions 38 can be formed in the peripheral area of the substrate outside of the memory array.

In one embodiment (Fig. 2), diffusion regions 38 can be formed prior to formation of conductive lines 28. Such permits the conductive lines to be formed over the diffusion regions so that the diffusion regions extend directly under conductive portions of the conductive lines. In another, more-preferred embodiment (Fig. 3), two individual diffusion regions 38a are formed after formation of conductive lines 28, and on each side thereof. A pair of isolation oxide regions 39 can be provided as shown. Individual diffusion regions 38, 38a-b are disposed operably proximate respective individual conductive line portions 40 and define areas which are comprised of a second-type dopant which is different from the first-type dopant comprising the substrate. Where substrate 26 comprises p-type dopant, diffusion regions 38, 38a-b comprise n-type dopant. Conversely, where substrate 26 comprises n-

type dopant, diffusion regions 38, 38a-b comprise p-type dopant. The diffusion regions and conductive line portions 40 collectively effectively define individual contact pads 42 with which electrical and physical connection is desired. The diffusion regions and substrate provide a pn junction which can be configured into a reverse-biased diode configuration during operation, as will become apparent below.

A layer of insulative material 44 is formed over substrate 26 including line portions 40 and diffusion regions 38, 38a-b. An exemplary material is borophosphosilicate glass. Contact openings 46 are formed through layer 44 and expose portions of individual contact pads 42. Contact openings 46 can overlap with individual conductive lines and their associated diffusion regions as shown. Conductive contacts 48 are formed or deposited within contact openings 46 and in electrical connection with the individual contact pads 42. In a preferred embodiment, conductive contacts 48 comprise metal such as tungsten, including metal alloys. In the illustrated example, conductive contacts 48 provide conductive material which is received over the conductive lines and interconnects the line with its associated diffusion region. Accordingly, material of contacts 48 electrically contacts both conductive lines 28 and their respective diffusion regions 38, 38a-b.

Referring to Fig. 4, individual conductive lines 28 have second conductive line portions 50 which are joined with respective first conductive line portions 40 and in electrical communication therewith. Individual conductive lines 28 have pitches P relative to respective next

adjacent lines. At least one, and preferably a plurality of the conductive lines have a pitch P between its first conductive line portion 40 and a next adjacent line which is substantially the same as a pitch between its second conductive line portion 50 and the next adjacent line. In the illustrated example, individual conductive lines 28 each have a lateral width dimension W away from its conductive line portion 40 which is substantially equivalent to the lateral width dimension of its conductive line portion 40. Preferably, the conductive lines have substantially equivalent lateral width dimensions.

Alternately considered, each conductive line has an average lateral width dimension W. Conductive line portions 40 have lateral width dimensions which are substantially equivalent to the average lateral width dimension of its associated conductive line. Such provides the conductive lines to have a generally uniform lateral width dimension along their respective entireties.

One advantage provided by the invention is that conductive lines 28 can be formed to have pitches which are more defined by minimum photolithographic feature sizes, without the lines having widened contact pads comprising material of the conductive lines. Thus, contact openings 46 can be formed over every other line (Fig. 4) along a generally straight line 52. There is no spacing-induced need to stagger the contact openings because the widened contact or landing pads can be eliminated.

Integrated circuitry formed in accordance with the inventive methods can provide a reverse-biased pn junction elevationally lower than one or more conductive lines, e.g. lines 30, 32, and 50. Electrical current may be provided through conductive lines 30, 32, and 50 and conductive material forming conductive contacts 48, with a reverse-biased pn junction between regions 38, 38a and substrate 26 being sufficiently reverse biased to preclude electrical shorting between conductive lines 30, 32 and 50, and substrate 26. Conventionally, in a DRAM, substrate 26 is biased to a negative voltage level V_{bb} on the order of 1 volt, and it is anticipated that voltage on contact via 48 is maintained in reverse bias, e.g. 0 volts. This allows for a reduction in wafer real estate which was formerly required to accommodate the widened contact pads (Fig. 1).

As an example, where substrate 26 comprises p-type material, the substrate can be provided at a voltage potential of -1 volt, and conductive contact 48 can be grounded to provide the desired reversed bias. Where substrate 26 comprises n-type material, the substrate can be biased at a voltage potential of around 4 volts, with conductive contact 48 being biased at around 2 volts to provide the desired reversed bias. Other advantages of the present invention include a reduction in circuit layout area as well as an increased number of contacts being provided in the same substrate wafer area.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical

features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.